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transistor and the non-volatile memory transistor, and wherein the second voltage-type transistor is positioned between the third voltage-type transistor and the first voltage-type transistor.

Please add new claim 30 as follows:

--30. (new) A semiconductor device as in claim 22, wherein

the first voltage-type transistor includes a gate dielectric layer having a first thickness,

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the second voltage-type transistor includes the gate dielectric layer formed from at least two insulation layers, the gate dielectric layer having a second thickness, and

the third voltage-type transistor includes a gate dielectric layer having a third thickness, wherein the second thickness is greater than the first thickness and the third thickness is greater than the second thickness.--

REMARKS

Claims 1-2, 4, 6-10, 12, 19, 22, 24, 26-27 and 29 have been amended and new claim 30 was added. Claims 1-30 are currently pending. Reexamination and reconsideration are respectfully requested.

Claims 1-11, 19-21 and 23 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 5,674,762 to See et al. ("See") in view of U.S. Patent No. 6,194,269 to Sung et al. ("Sung"). The rejection is respectfully traversed.

Claims 1-2, 4, 6-10 and 19 have been amended. Applicant respectfully submits that the Examiner cited no specific portion of the art that describes or suggests a device as recited in claim 1, which recites in part "the third transistor region including a third voltage-type transistor that operates at a third voltage level that is higher than the first and second voltage levels, wherein the device includes a first thermally oxidized gate dielectric layer formed in the second transistor region, and . . . a second thermally oxidized gate dielectric layer formed in the first transistor region and the second transistor region, wherein the second thermally oxidized gate dielectric layer in the second transistor region is positioned on the first thermally oxidized gate dielectric layer." Accordingly, the rejection of claim 1 over See in view of Sung should be withdrawn.

Claims 2-11 depend from claim 1 and their rejection over See in view of Sung should be withdrawn for at least the same reasons as claim 1. In addition, with respect to claim 2, applicant respectfully submits that the Examiner cited no portion of the art that describes or suggests a device "wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, and wherein the second thermally oxidized gate dielectric layer is also formed in the third transistor region as one of the at least three insulation layers" as recited in claim 2, as amended. In addition, with respect to claim 6, applicant respectfully submits that the Examiner cited no portion of the art that describes or suggests a device in which "the third voltage-type transistor has a gate insulation layer formed from three insulation layers, and the gate insulation layer of the third voltage-type transistor has an identical thickness as the intermediate insulation layer of the non-volatile memory transistor" as recited in claim 6, as amended. Applicant also respectfully submits claims 7-10, which depend from claim 6, are not suggested by the Examiner's citations to the art for at least the same reasons as claim 6.

Applicant respectfully submits that the Examiner cited no portion of the cited art that suggests all of the elements of claim 19, including "wherein the non-volatile memory transistor intermediate insulation layer has a thickness that is identical to that of the gate insulation layer of the third voltage-type transistor." Accordingly, the rejection of claim 19 and its dependent claims 20-21 and 23 should be withdrawn.

Claims 1-23 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 5,153,143 to Schlais et al. ("Schlais") in view of U.S. Patent No. 4,651,406 to Shimizu ("Shimizu"). The rejection is respectfully traversed.

Applicant respectfully submits that the proposed combination of references would not be made by one of ordinary skill in the art. The Examiner stated at page 3 of the Office Action that "with respect to the Schlais et al. references, the transistor 64 would be expected to operate at a higher voltage than the CMOS transistors, since the transistor 64 is associated with the memory device which operates at higher voltages than the CMOS transistors." However, applicant notes that Schlais states that "the EEPROM is designed so that it is programmable at a low voltage which is compatable with the low voltages typically used with the CMOS circuit." Schlais et al. Abstract. Thus, it appears that Schlais teaches away from the motivation suggested by the Examiner and thus one of ordinary skill would not make the combination suggested by the

Examiner. Accordingly, for at least the above reason, the rejection of claims 1-23 over Schlais et al. in view of Shimizu et al. should be withdrawn.

The Examiner also referred to the previous Office Action (paper no. 4), which includes various comments concerning the obviousness of features in various claims. Applicants respectfully disagree with the Examiner's obviousness conclusions. The discussion above has directly addressed some of those comments and the Examiner's other comments are deemed moot at this time in view of the above response.

Applicant has rewritten claims 12 and 22 in independent form, with minor changes for clarity (and not in response to any rejection) to claim 12 as rewritten.

Applicant thanks the Examiner for indicating the claims 24, 26-27 and 29 contained allowable subject matter. These claims have been rewritten in independent form to include the limitations of the base claims and any intervening claims.

New claim 30, dependent from claim 22, has been added. Support for the new claim may be found throughout the specification and original claims. No new matter was added.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 1-30 are in condition for allowance. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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March 20, 2003

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Box RCE, Commissioner for Patents, Washington, D.C. 20231 on March 20, 2003.

Alan S. Raynes — March 20, 2003

Alan S. Raynes **(Date)**

Version With Markings to Show Changes Made

The specification at page 1, lines 6-13 was amended as follows:

[The copending and commonly assigned patent application having Serial No entitled "Methods for Manufacturing Semiconductor Devices Having a Non-Volatile Memory Transistor", with Tomoyuki Furuhata and Atsushi Yamazaki listed as inventors, with docket no. 15.15/5049,] U.S. Patent No. 6,429,073 is hereby incorporated by reference in its entirety. [The copending and commonly assigned patent application entitled "Non-Volatile Semiconductor Memory Devices", with Tomoyuki Furuhata and Atsushi Yamazaki listed as inventors, with docket no. 15.16/5050,] U.S. Patent No. 6,522,587 is hereby incorporated by reference in its entirety. Japanese patent application no. 11-177146, filed June 23, 1999, is hereby incorporated by reference in its entirety.

Claims 1-2, 4, 6-10, 12, 19, 22, 24, 26-27 and 29 have been amended as follows:

1. (amended) A semiconductor device comprising a memory region, first, second and third transistor regions including field effect transistors that operate at different voltage levels,

the memory region including a split-gate non-volatile memory transistor,

the first transistor region including a first voltage-type transistor that operates at a first voltage level,

the second transistor region including a second voltage-type transistor that operates at a second voltage level, and

the third transistor region including a third voltage-type transistor that operates at a third voltage level that is higher than the first and second voltage levels,

wherein the device includes a first thermally oxidized gate dielectric layer formed in the second transistor region, and

wherein the device includes a second thermally oxidized gate dielectric layer formed in the first transistor region and the second transistor region, wherein the second thermally oxidized

gate dielectric layer in the second transistor region is positioned on the first thermally oxidized gate dielectric layer

[wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers, and includes gate insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed].

2. (amended) A semiconductor device according to claim 1, wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, and wherein the second thermally oxidized gate dielectric layer is also formed in the third transistor region as one of the at least three insulation layers [includes an insulation layer that is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed].

4. (amended) A semiconductor device according to claim 3, wherein the second outermost layer that contacts the control gate is formed in the same step in which the [gate insulation layer of the first voltage-type transistor is formed] second thermally oxidized gate dielectric layer is formed.

6. (amended) A semiconductor device according to claim 5, the third voltage-type transistor has a gate insulation layer formed [in the same step in which] from three insulation layers, and the gate insulation layer of the third voltage-type transistor has an identical thickness as the intermediate insulation layer of the non-volatile memory transistor [is formed, the gate insulation layer of the third voltage-type transistor being formed from at least three insulation layers].

7. (amended) A semiconductor device according to claim 6, wherein the first voltage-type transistor has a gate insulation layer formed from the second thermally oxidized layer and has [having] a thickness of 3 – 13 nm.

8. (amended) A semiconductor device according to claim 7, wherein the second voltage-type transistor has a gate insulation layer that includes the first thermally oxidized layer and the second thermally oxidized layer and has [having] a thickness of 4 – 15 nm.

9. (amended) A semiconductor device according to claim 8, wherein the third voltage-type transistor has a gate insulation layer that includes the second thermally oxidized layer and at least two additional layers and has [having] a thickness of 16 – 45 nm.

10. (amended) A semiconductor device according to claim 9, wherein the second thermally oxidized gate dielectric layer is also formed in the memory region, wherein the non-volatile memory transistor has an intermediate insulation layer that includes the second thermally oxidized layer [having a thickness of 16 – 45 nm].

12. (amended) A semiconductor device [according to claim1,] comprising a memory region and first, second and third transistor regions including field effect transistors that operate at different voltage levels;

the memory region including a split-gate non-volatile memory transistor,

the first transistor region including a first voltage-type transistor that operates at a first voltage level;

the second transistor region including a second voltage-type transistor that operates at a second voltage level; and

the third transistor region including a third voltage-type transistor that operates at a third voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed; and

wherein the first voltage level that operates the first voltage-type transistor is 1.8 – 3.3 V, the second voltage level that operates the second voltage-type transistor is 2.5 – 5 V, and the third voltage level that operates the third voltage-type transistor is 10 – 15 V.

19. (amended) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

[wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers]

wherein the non-volatile memory transistor intermediate insulation layer has a thickness that is identical to that of the gate insulation layer of the third voltage-type transistor.

22. (amended) A semiconductor device [as in claim 19,] comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers; and

wherein the first voltage level is in the range of 1.8 to 3.3 V, the second voltage level is in the range of 2.5 to 5 V, and the third voltage level is in the range of 10 to 15 V.

24. (amended) A semiconductor device [as in claim 21,] comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate; and

wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, wherein the at least three insulation layers of the third voltage type transistor are identical in composition to the at least three insulation layers of the intermediate insulation layer of the non-volatile memory transistor.

26. (amended) A semiconductor device [as in claim 25,] comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation

layer contacts the control gate;

wherein the first voltage-type transistor has a gate insulation layer having a thickness that is less than that of the second voltage-type transistor, and the second voltage-type transistor has a gate insulation layer having a thickness that is less than that of the third voltage type transistor; and

wherein the non-volatile memory transistor intermediate insulation layer has a thickness that is identical to that of the gate insulation layer of the third voltage-type transistor.

27. (amended) A semiconductor device [as in claim 25,] comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate;

wherein the first voltage-type transistor has a gate insulation layer having a thickness that is less than that of the second voltage-type transistor, and the second voltage-type transistor has a gate insulation layer having a thickness that is less than that of the third voltage type transistor; and

wherein the first voltage-type transistor is positioned adjacent to the non-volatile memory transistor, the second voltage-type transistor is positioned adjacent to the first voltage-type transistor, and the third voltage-type transistor is positioned adjacent to the second voltage-type

transistor, wherein the first voltage type transistor is positioned between the second voltage type transistor and the non-volatile memory transistor, and wherein the second voltage-type transistor is positioned between the third voltage-type transistor and the first voltage-type transistor.

29. (amended) A semiconductor device [as in claim 28,] comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate;

wherein the first voltage-type transistor operates at a lower voltage range than that of the second voltage-type transistor, and the second voltage-type transistor operates at a lower voltage range than that of the third voltage-type transistor; and

wherein the first voltage-type transistor is positioned adjacent to the non-volatile memory transistor, the second voltage-type transistor is positioned adjacent to the first voltage-type transistor, and the third voltage-type transistor is positioned adjacent to the second voltage-type transistor, wherein the first voltage type transistor is positioned between the second voltage type transistor and the non-volatile memory transistor, and wherein the second voltage-type transistor is positioned between the third voltage-type transistor and the first voltage-type transistor.